

TECHNICAL DESCRIPTION

# Model BE-64

Bus Emulator/Word Generator

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# 1. INTRODUCTION

The BE-64 is a C size VXI card which houses the digital resources required in digital test and troubleshooting applications. The BE-64 may be software configured to handle applications ranging from basic word generator requirements to the most sophisticated microprocessor or bus structured interface requirements

## 1.1. Bus Emulation

Bus Emulation is a technology which enables an engineer to simulate all the signal characteristics of a given interface. Programmable bus emulation allows the user to software configure the programmable bus emulator to simulate literally an infinite number of digital interfaces.

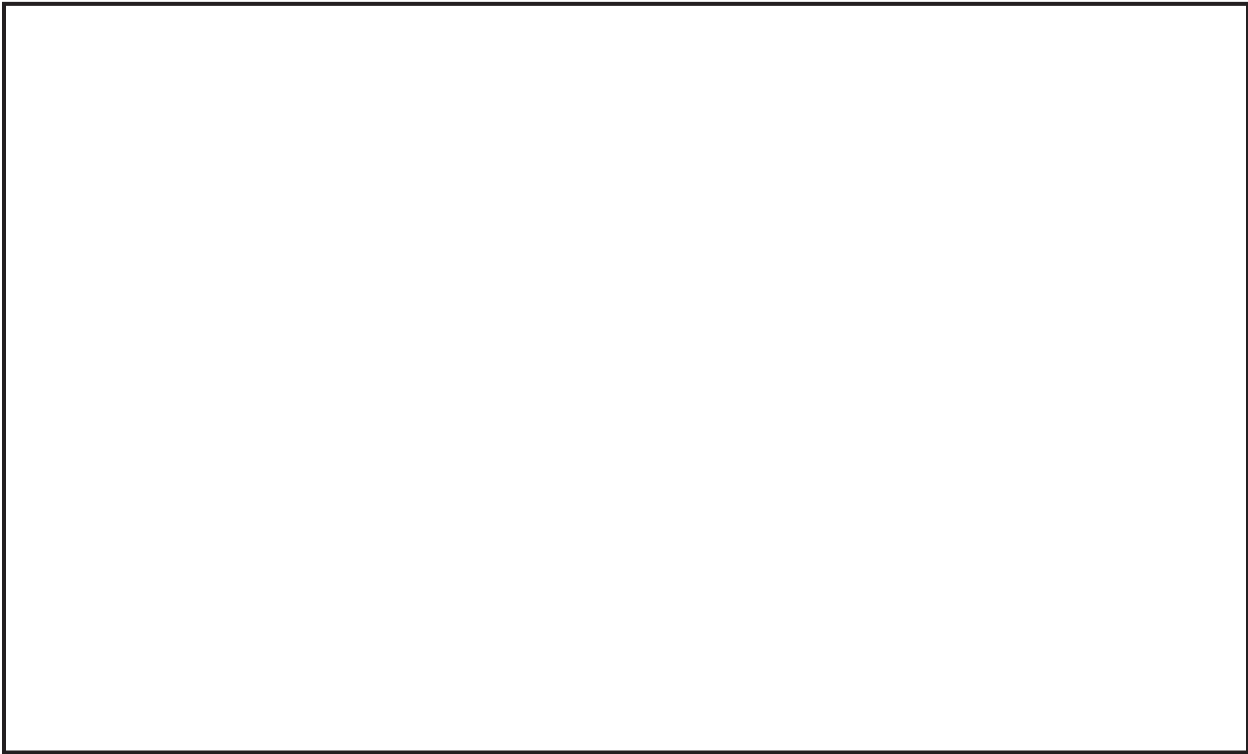
The term 'bus emulation' generally implies microprocessor and/or bus structured interfaces. However, to infer that Talon's programmable bus emulator simulates only these categories of interfaces would be a substantial understatement. While the programmable bus emulator is ideally suited to simulate a VME bus, Multibus, SCSI bus, 80486, or 68030 bus structured interface, the emulator can also simulate almost any digital interface; interfaces such as serial communication interfaces, state sequencer interfaces or any user defined digital interface. Indeed, most digital interfaces can be considered to be a subset of a bus structured interface.

## 1.2. Bus Emulation Testing

Bus Emulation Testing is a test method in which the unit under test (UUT) is exercised, in real time, through all of its functions. This is accomplished by precisely simulating all the interfaces into and out of the UUT as well as transferring functional data to/from the UUT. Successful bus emulation testing requires independent bus emulators for each interface resident on the UUT.

Figure 1 depicts a typical UUT. The UUT has two interfaces, a VME interface and a SCSI bus interface. Successful test of the UUT requires two bus emulators, each providing a real time simulation of the address, data, and control lines of the respective bus, as well as the ability to transmit and receive functional data to/from the UUT.

This UUT also incorporates a 68020 microprocessor. If it is desirable to emulate the 68020, a third bus emulator would be installed to simulate this function. The UUT would then be exercised, in real time, through all its functions.



**Figure 1**

### 1.3. BE-64 I/O Signal Overview

- 64 I/O Channels x 32K bits/chan (Address and Data fields or Word Generator Data; maximum data rate = 25 MHz)
- 12 Output Programmable Timing and Control Signals; maximum output rate = 50 MHz
- 3 Input Programmable Timing and Control Signals; maximum input rate = 50 MHz
- 6 Input External Field Control Signals; maximum input rate = 25 MHz
- 24 Programmed Input/Output Signals; data rate defined by data transfer rate of VXI controller
- 30 miscellaneous timing and control signals required for exact simulation of various microprocessors and compatible signals for parallel to serial word generator converter card
- 1 Clock Out; frequency = 50 MHz, 20 MHz, or 10 MHz
- 1 Clock input; maximum frequency = 50 MHz
- All signals TTL compatible

## 2. WORD GENERATOR OVERVIEW

Since “bus emulator” is a relatively new technology, this document will first describe the basic concept of a word generator. This will establish a baseline for the bus emulation description. The reader should note that the BE-64 module is capable of executing all the concepts which are described in this document.

A basic digital word or pattern generator is composed of a number of I/O channels where the group of channels define a single “word”. Each channel is further described by a serial data stream. When the Talon BE-64 is looked at from this viewpoint, its word generator capacity is 64 I/O channels with a 32K word depth, fig. 2.

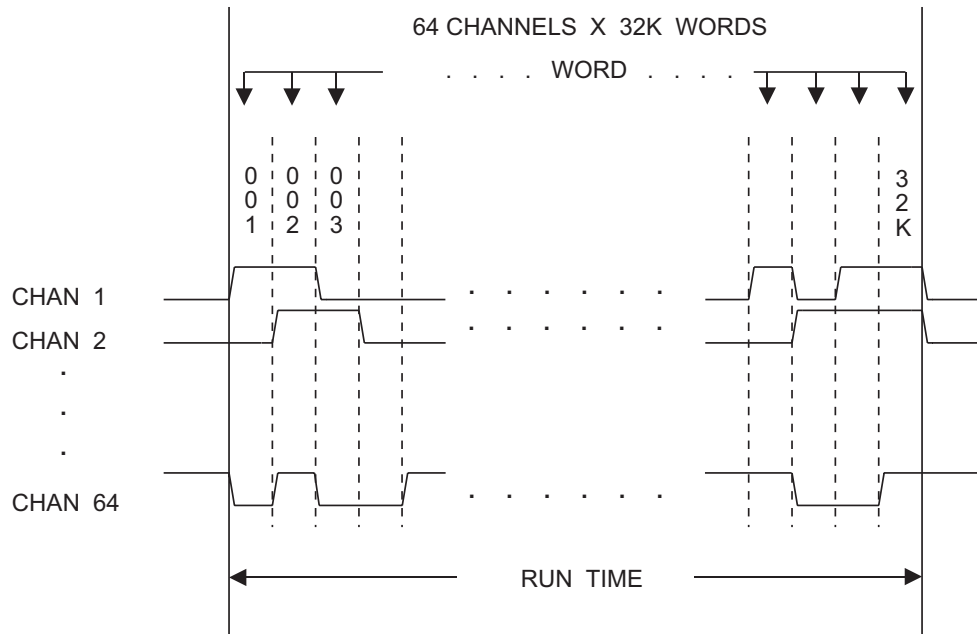
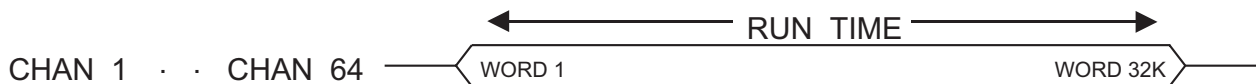


Figure 2.

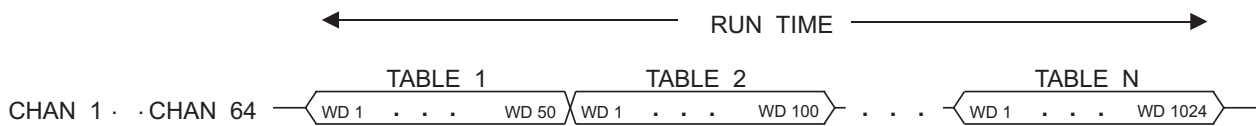
In a run mode, the data would be output across the channels starting with word 1 and continuing through word 32K, generating a continuous stream of data. The time required to execute the entire table is referred to as RUN TIME.

For illustrations' sake we will consolidate fig. 2 into the abbreviated fig. 3 below.



## 2.1. Tables

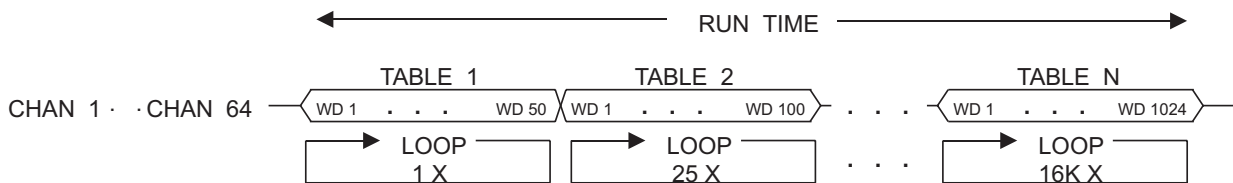
When using a word generator, it is desirable to subdivide the entire word generator memory into smaller sections, each section dedicated to a specific UUT operation. The BE-64 refers to the divided memory as tables, fig. 4. The BE-64 can be divided into as many as 100 tables. The table length can be individually configured from 1 word to the full 32K memory depth. The RUN TIME is the time required to execute all the tables in the sequence. The execution of the tables is continuous with zero dead time between tables.



**Figure 4.**

## 2.2. Table Looping

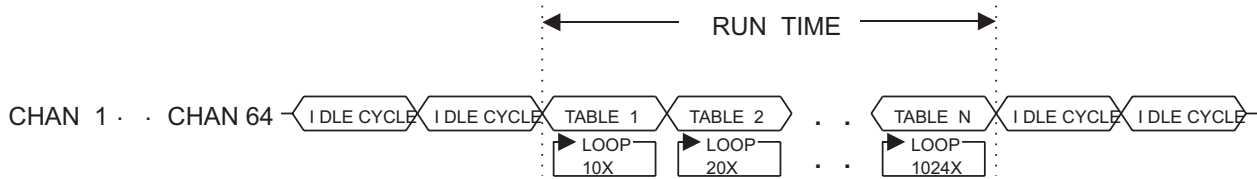
The ability to individually loop the tables is often desirable in order to create a repeating stimulus to the UUT. The BE-64 allows individual tables to be looped from 1 to 64K times, fig. 5. In addition, tables can be looped indefinitely with the stop or exit from a loop directed by the VXI Slot 0 Controller. Exiting an indefinite loop will cause the interrupted loop to complete its cycle and move to the start of the next table. Again, the RUN TIME is the amount of time to complete the entire sequence of tables.



**Figure 5.**

### 2.3. Idle Cycle

The BE-64 incorporates a unique function which is not found on present data generators, this feature being the idle cycle. The idle cycle allows the user to define a timing and data sequence prior to and after the "run time", fig. 6. This idle cycle can be programmed such that no signal activity is seen by the UUT, or a complete repetitive timing cycle with associated data patterns could be defined.

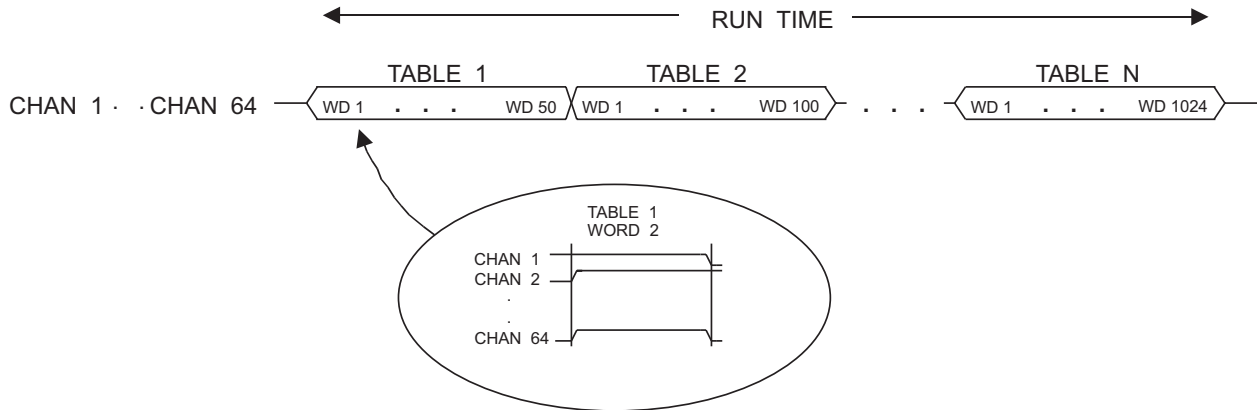


**Figure 6.**

One of the key functions of the idle cycle is the ability of the VXI controller to download new data tables, loop count values, and sequence of operation while the idle sequence is running. This feature enables a UUT to continue to receive required timing signals while new data is defined for the next operation.

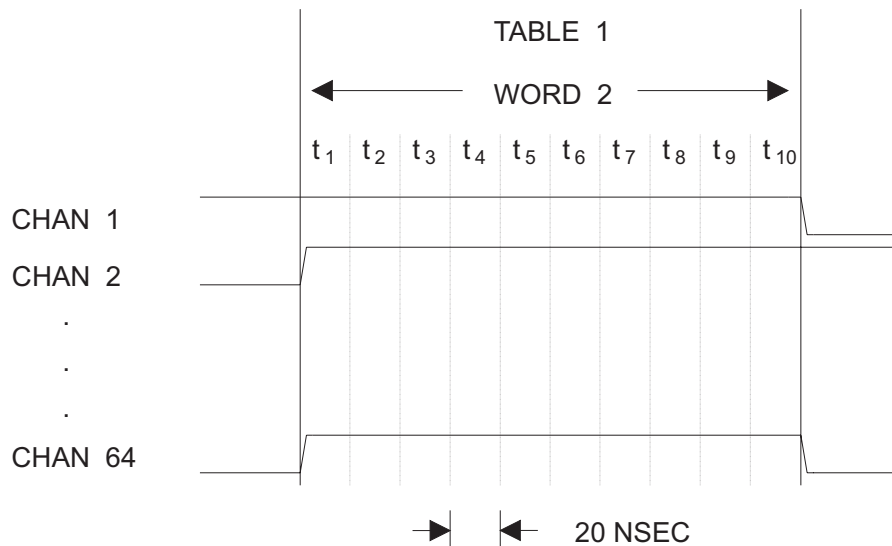
### 3. BUS EMULATION OVERVIEW

In general, word generator parameters describe the sequencing of data from one word to the next, and from one table of data to the next table. Bus emulation describes what happens “inside” each word. For example, let's take a look at what's happening inside word 2 of table 1, fig. 7.



**Figure 7.**

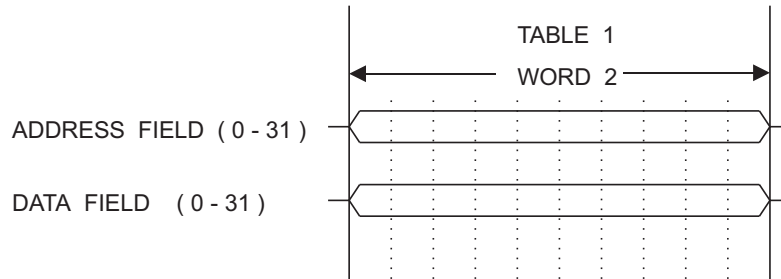
The BE-64 allows an individual word to be divided into timing increments with resolution of 20 nsec per increment. Fig. 8 depicts word 2 of table 1, where word 2 has a total period of 200 nsec



**Figure 8.**

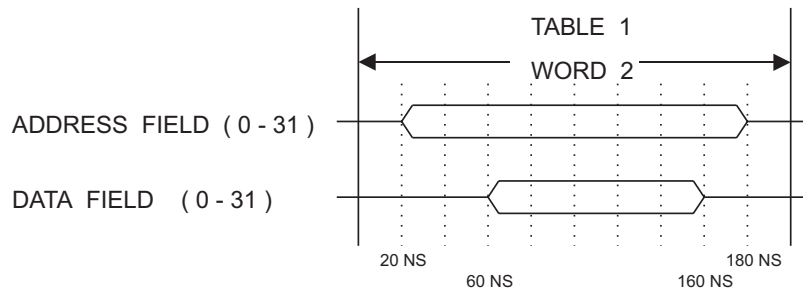
### 3.1. Fields

Figure 9 again depicts word 2, table 1, however this figure we will break up the 64 channels into two fields, an address field and a data field. This configuration will allow our example to follow a more traditional bus structure interface.



**Figure 9**

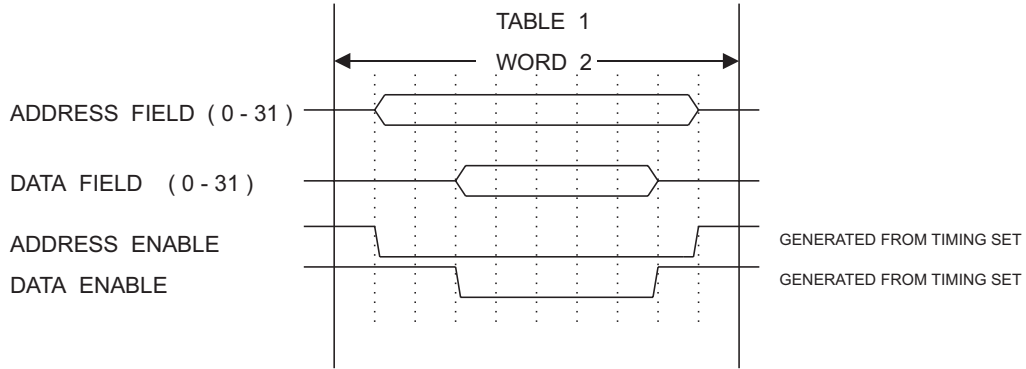
In most applications, the signals comprising a word in a field are not active during the entire word period. As shown in fig. 10, the address field period may be active from 20 nsec ( $t_1$ ) to 180 nsec ( $t_9$ ), while the data field is active from 60 nsec ( $t_3$ ) to 160 nsec ( $t_8$ ).



**Figure 10.**

### 3.2. Field Timing

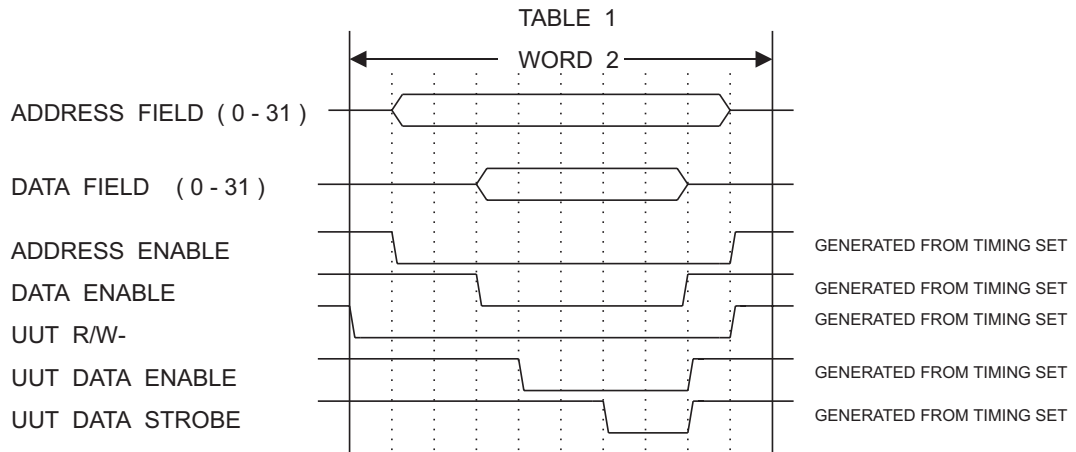
In order to activate the “bus signals” depicted in Figure 10 the busses require control signals. In particular, they require an ADDRESS ENABLE and DATA ENABLE signal, fig. 11. These signals are generated from a separate timing generator, nomenclated the ” timing set”.



**Figure 11.**

### 3.3. Timing Signals

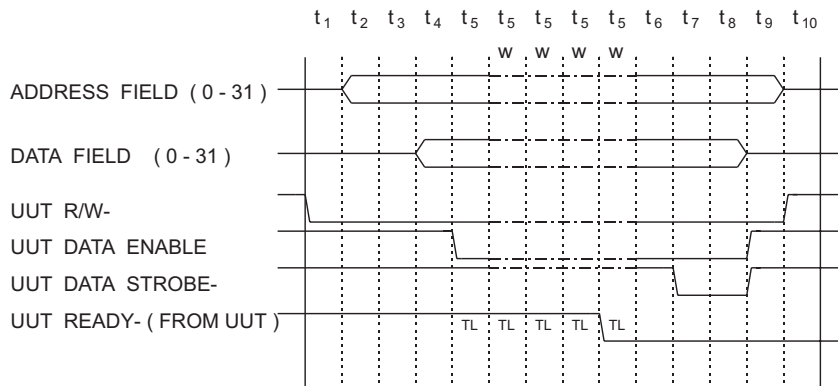
Typically, the UUT requires additional control signals which further define the “bus cycle”. Example 12 describes a UUT R/W-, a UUT Data Enable and a UUT Data Strobe signal. These signals are also generated by the BE-64 timing set.



**Figure 12**

Once active data has been placed on the data bus and the data enable signal has been asserted, there must be a means to determine that the UUT is ready for data. The timing set must have the ability to test the UUT READY signal and enter a "Wait" state until the test condition is true. This sequence is often referred to as a "handshake" sequence.

Fig. 13 indicates that the timing set will remain in state  $t_4$  until the UUT READY- signal goes low. Once the UUT READY- = Low condition is met, the timing set will continue. If the test condition does not occur in a specified time, a time-out condition will force the continuation of the timing set and inform the VXI controller that a time-out occurred. The time-out logic can be disabled, which in turn will cause the BE-64 to remain in state  $t_4$  until commanded to complete by the VXI controller.

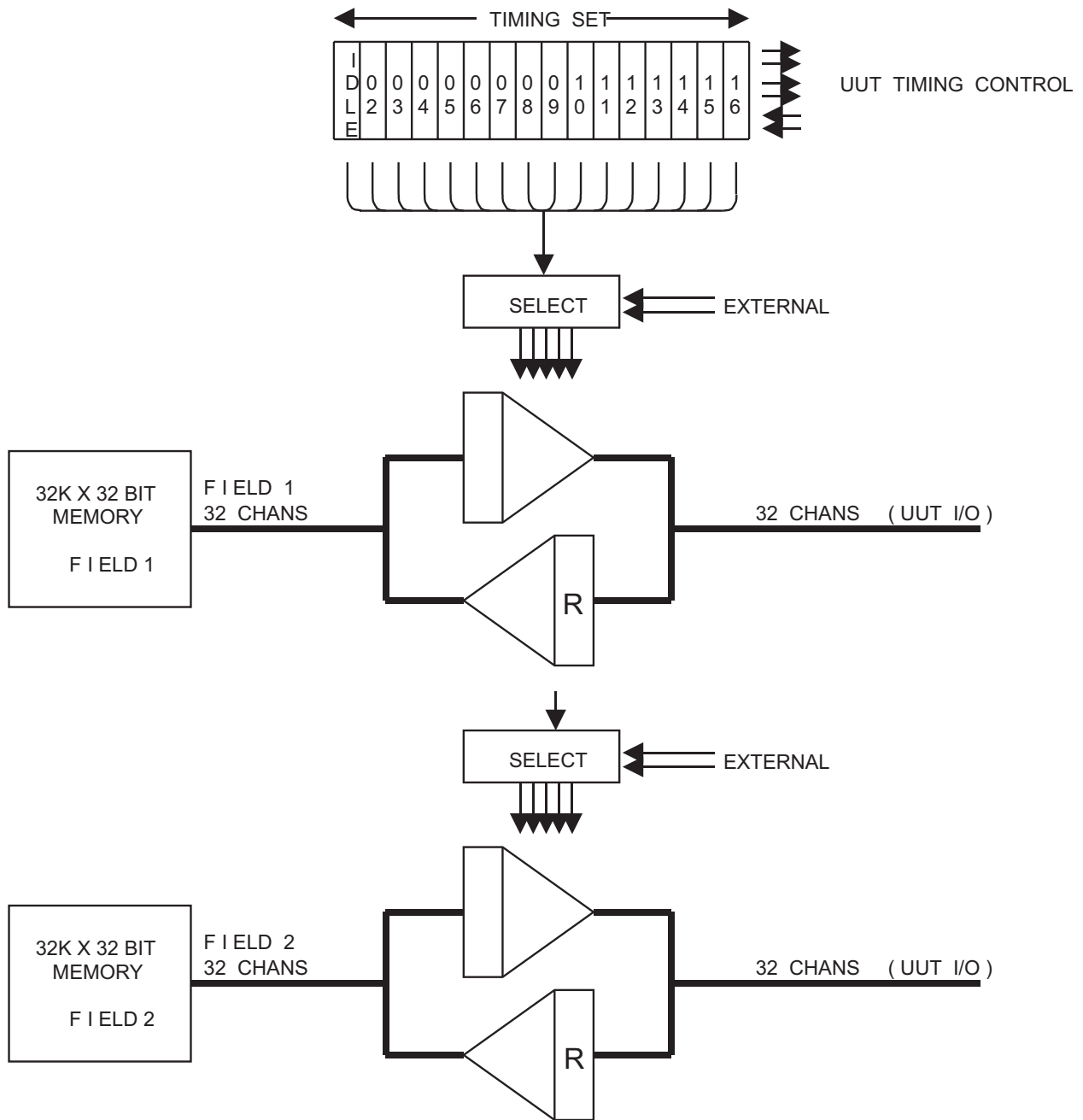


**Figure 13.**

The BE-64 incorporates 16 timing sets, each timing set programmed to simulate a particular bus cycle type or UUT timing cycle.

### 3.3.1. Field Timing Overview

Fig 14 depicts the sixteen timing set generates all the timing and control signals required by the UUT as well as defines the control signals to the field I/O buffers. In addition, the timing set increments the field memories after the completion of the timing set cycle.

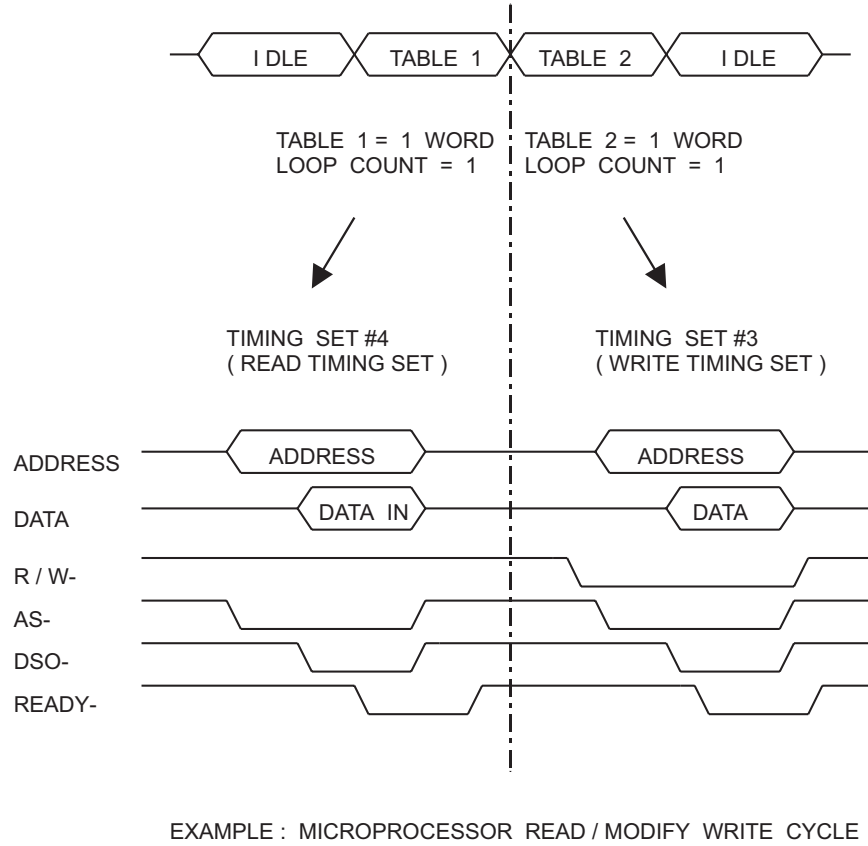


**Figure 14.**

Each timing set incorporates from 2 to 256 cells, each cell being 20 nsec, 50 nsec, 100 nsec, or a period defined by the external clock. Fig. 24, section 4.4.3 defines the timing set signals.

### 3.3.2. Read/Modify Write Example

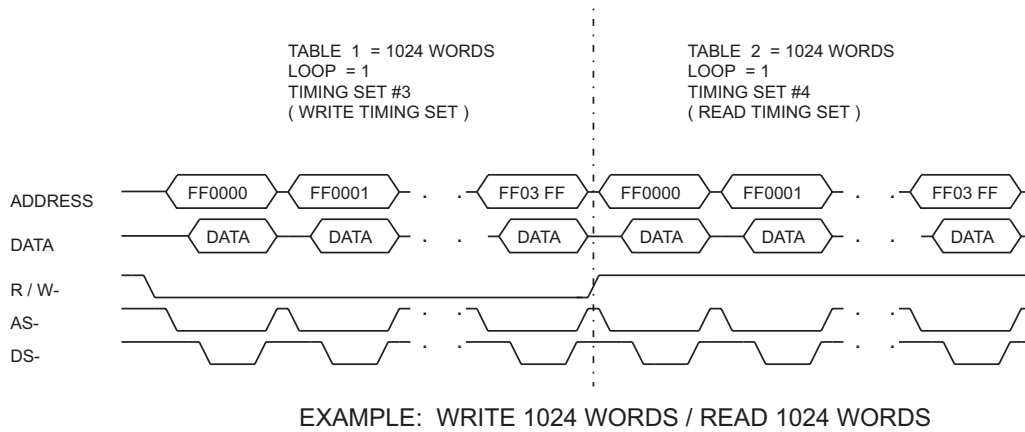
Fig. 15 depicts a typical example, the simulation of a Read/Modify Write microprocessor bus cycle. To implement this simulation, table 1 would be setup with one word, where field 1 is loaded with desired address value. Table 2 is also set to 1 word with both an address and data value specified. Timing set #4 would be programmed for the Read cycle, and timing set #3 programmed for the Write cycle.



**Figure 15.**

### 3.3.3. Write Block/Read Block Example

Fig. 16 depicts an example in which the BE-64 simulates 1024 write cycles followed by 1024 read cycles.



**Figure 16**

### 3.4. Field Control

Each timing set must also define the type of transfer which is being executed for each field (FIELD1, FIELD2). The two fields operate in an identical fashion, however each field is independent of the other. For example, one field could be in the output mode while the other is the input mode. In our examples above, the address field is output while data may be either input or output.

#### 3.4.1. Field Direction

Each timing set (1 of 16) specifies the field direction to be either input, output, or controlled by an external signal.

When set to OUTPUT mode, the present word from the 32K x 32 bit memory is available for output to the 32 UUT I/O channels, fig. 17.

When set to the INPUT mode, the present data on the UUT I/O channels may be strobed into the input register, fig. 17 and subsequently transferred to the field memory.

# SELECT FIELD DIRECTION

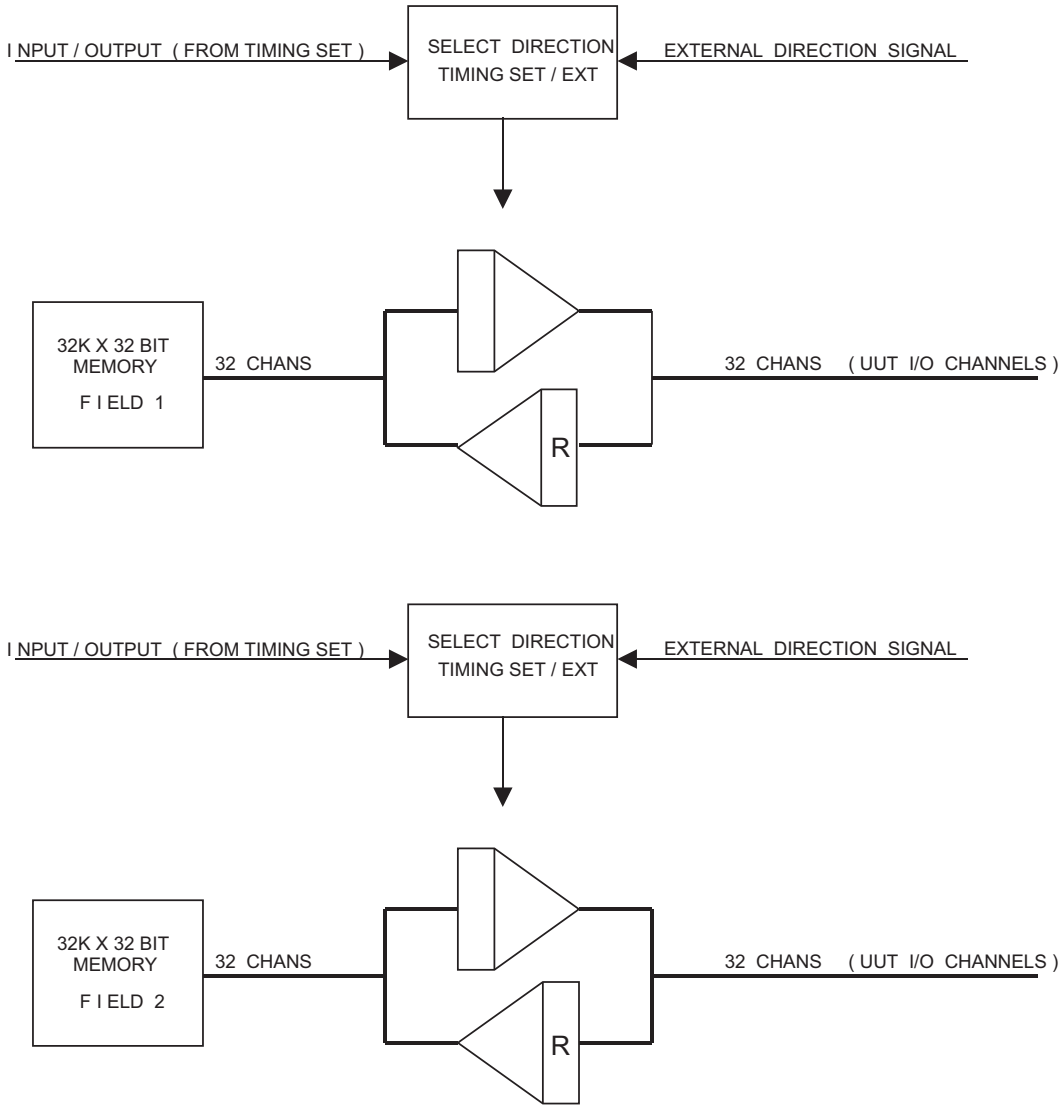


Figure 17.

### 3.4.2. Output Fields

Fields set to the OUTPUT mode may be registered or not, fig. 18. If registered, the output register (R) is strobed by the STROBE FIELD signal defined in the timing set, fig. 19.

If not registered, the data may be passed unobstructed from the field memory to the UUT I/O lines.

#### FOR OUTPUT FIELDS

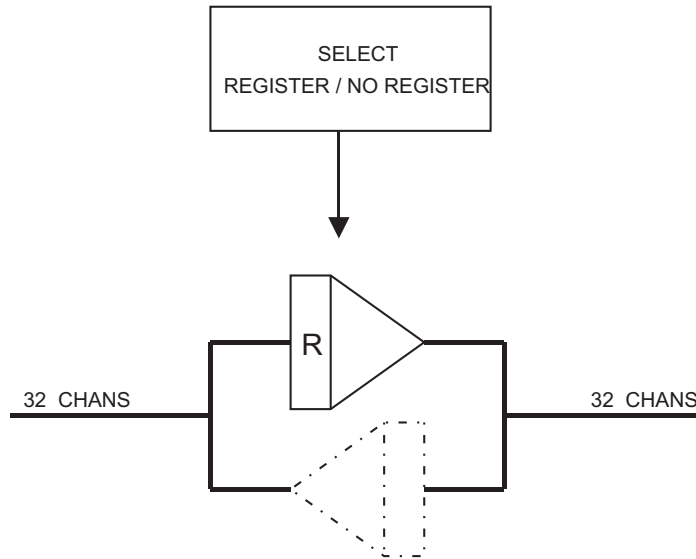


Figure 18.

#### FOR OUTPUT FIELDS WITH REGISTER

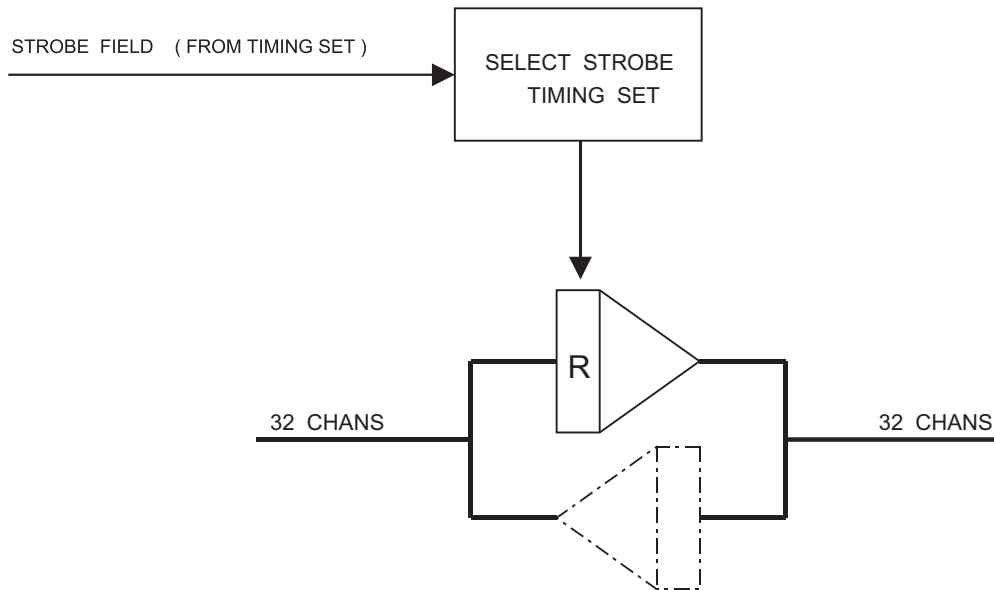
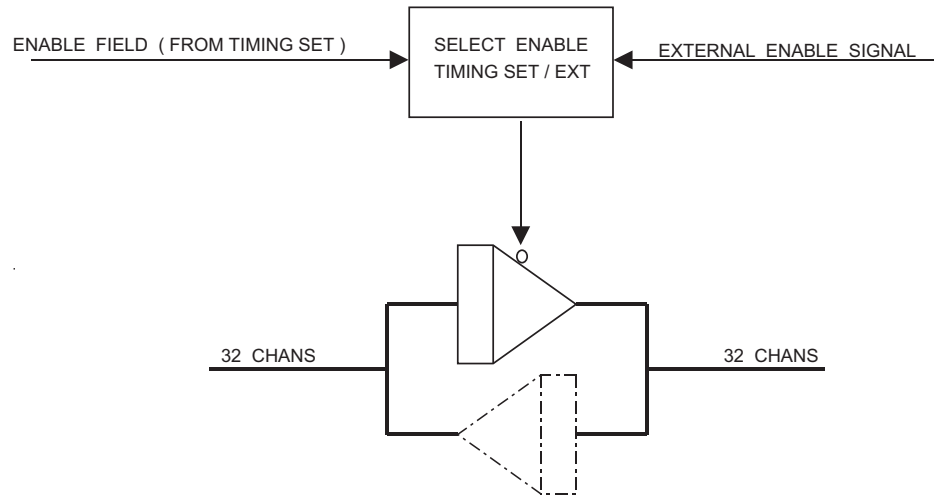


Figure 19

Both registered and nonregistered output requires an enable signal. This signal enables the I/O lines to follow either the register data (registered output) or the field memory (non registered). The enable signal can be selected to be the ENABLE FIELD signal generated by the timing set or an EXTERNAL ENABLE signal, fig. 20. When the enable signal is not true, the field data is in the tri-state condition.

### FOR OUTPUT FIELDS

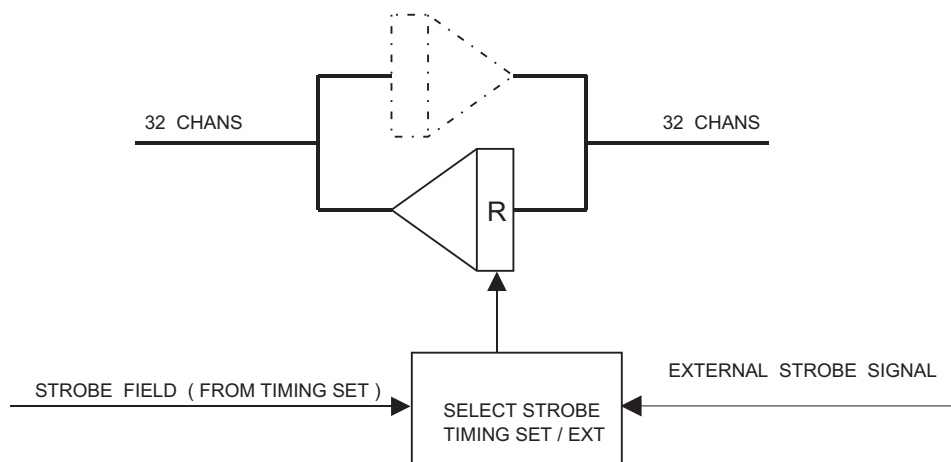


**Figure 20.**

### 3.4.3. Input Fields

When FIELDS are set to the input mode, the timing set must select an input strobe either from the timing set (STROBE FIELD) or from an EXTERNAL STROBE signal. The strobe signal must occur after the beginning of the timing set ( $t_0$ ) and prior to the last cell of the timing set. The strobed data is transferred into the 32K x 32 bit field memory during the last cell of the timing set.

### FOR INPUT FIELDS



**Figure 21.**

### 3.5. Sequence Overview

Fig. 22 depicts the overall BE-64 timing. The following sequence assumes the timing set memories and field data memories have been downloaded by the VXI controller.

In the quiescent state the BE-64 is executing the IDLE sequence. This includes the IDLE timing set as well as an idle field table (the idle table may be from 1 word to 32K words).

Next, the VXI controller would define a sequence of operations. The overall sequence can be from 1 sequence to 16 sequences.

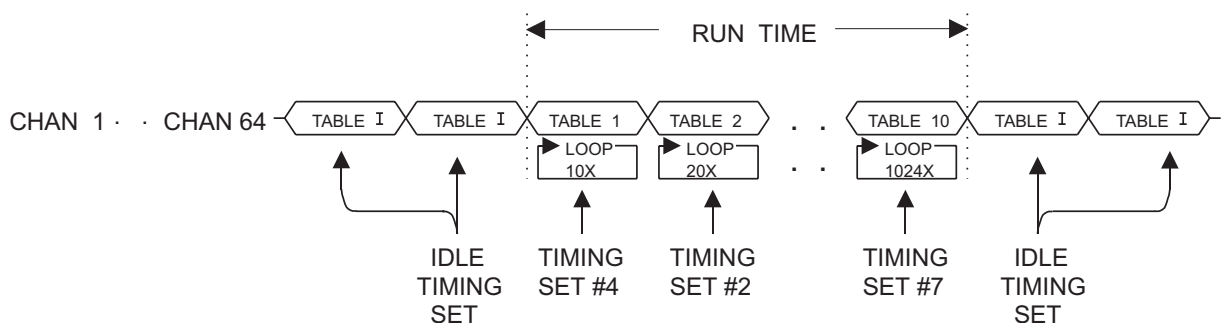
SEQUENCE 1 = TIMING SET4, TABLE1, LOOP COUNT = 10.  
 SEQUENCE 2 = TIMING SET2, TABLE2, LOOP COUNT = 20.  
 . . . . .  
 SEQUENCE N = TIMING SET7, TABLE10, LOOP COUNT = 1024.

(Tables 1,2,10 include table length)

Once the overall sequence is defined, the VXI controller can start the sequence. Upon detection of the last timing set bit and the last word of the Idle sequence, the BE-64 steps to Sequence #1, selecting the respective timing set, table #, and loop count. There is zero delay while changing timing sets and data tables.

The BE-64 remains in Sequence #1 until the last loop, last word of the table, and the last bit of the timing set is detected. At this time the next sequence is accessed or the BE-64 returns to the Idle sequence (i.e. total sequence is complete). In either case, again there is zero delay while changing timing sets and data fields.

When complete, the VXI controller can interrogate the input memories, request CRC's to be generated on the input memories, execute a host of other commands, including the execution of another sequence of operations.



**Figure 22**

**BE-64 BLOCK DIAGRAM DESCRIPTION**  
Fig. 23 depicts the block diagram of the BE-64 module. This diagram consists of a 68010 microprocessor, a VXI message based interface, the programmed I/O logic and the bus emulator logic.

#### 4.1. 68010 Microprocessor

The 68010 microprocessor performs the following functions.

1. Performs power-up self test.
2. Receives, parses and interprets VXI commands.
3. Processes VXI commands and converts commands into an appropriate digital format compatible with the bus emulator logic.
4. Executes VXI macro-commands such as UUT RAM and ROM test.
5. Calculates CRC's on field memories such that a "Learn UUT" function can be executed.

#### 4.2. VXI Interface

The VXI interface is a message based interface conforming to the SCPI Standard, Rev. 1991. The description of this interface is contained in section 6.0, BE-64 VXI Command Description.

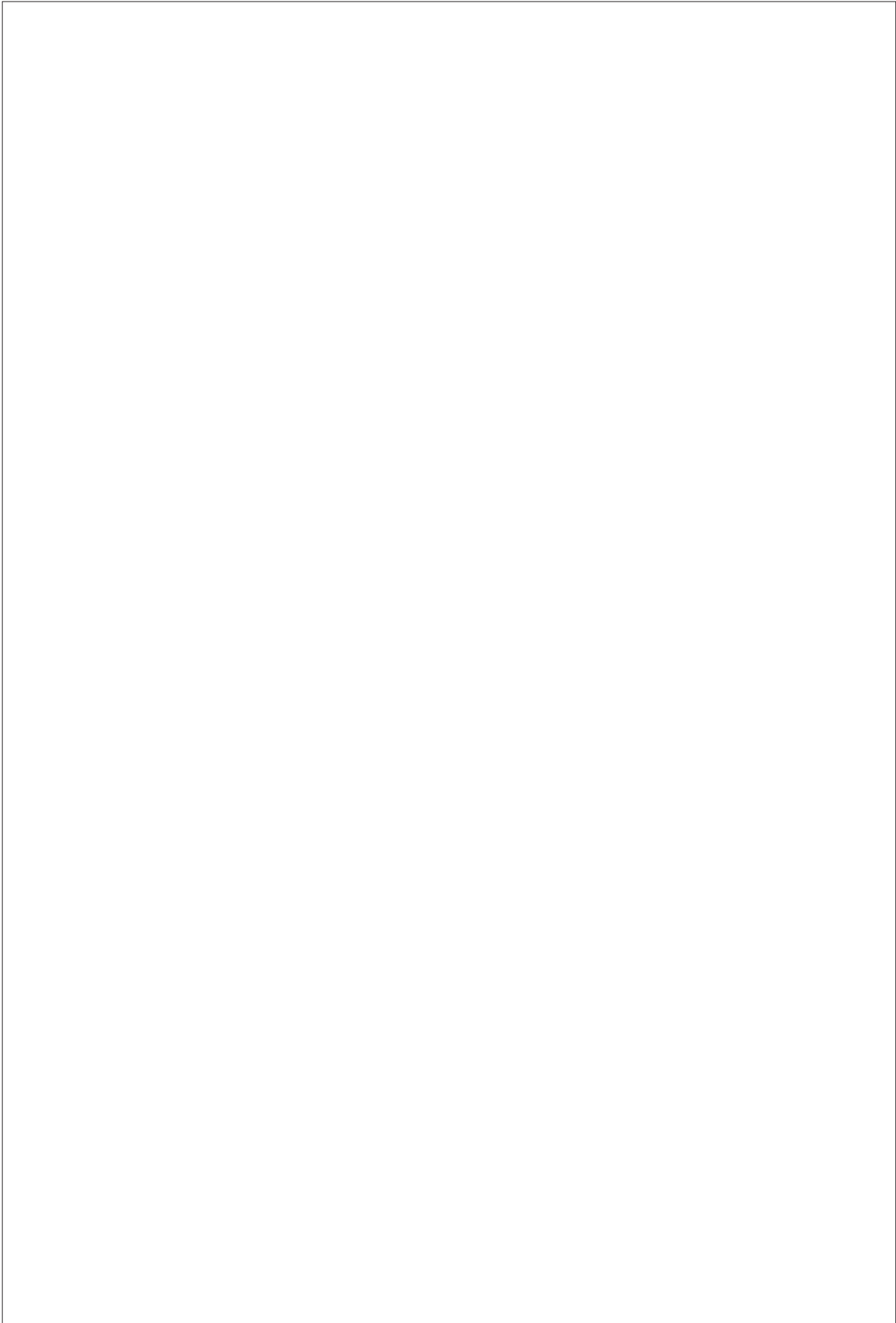
#### 4.3. Program I/O

The Program I/O logic consists of three 8 bit registers. Two of the registers (PIO1, PIO2) can be configured as either input or output while the third register (OUT 0-7) is output only (reference section 5.1, Program I/O).

A VXI command can discretely set, reset, or sense any bit in the PIO1 or PIO2 registers.

The third register, OUT0 thru OUT7, fig. 1, can be configured to be either an output register, or configured as a counter. When set to the output register mode, a VXI command can directly set or reset each bit of the register. When configured as a counter, a VXI command can define a first count address. The first count address is saved and may be used to load the counter later when the terminal count is detected. The counter controls are defined in section 5.1.2.

The counter logic has been designed such that the control signals are compatible with the proprietary control signal shown on the timing set, fig. 23. With the proper connection, the counter can be used to generate address bits A16-A23 of a UUT memory address bus (A0-A15 is generated by Field 1). This enables memory card testing where 16 megabyte of RAM can be continuously accessed with zero delay between memory address locations.



**Figure 23**

## 4.4. Bus Emulator Logic

The bus emulator logic consists of field 1 and field 2 drivers, the field memory addressing logic, the timing set logic and the sequence logic.

Prior to any VXI commands defining a UUT test function (for example, transfer an address, data and control signals to simulate a write cycle to the UUT) several memories must be loaded. These memories can be directly addressed and loaded via the VXI bus or they can be loaded via VXI message commands

### 4.4.1. Field Timing Set Memories

The BE-64 incorporates two field memories, each being 32K words by 32 bits per word. Typically, these two fields would be used to simulate an address and data bus of the UUT, however they may be used to simulate any type data bus. In addition, they may be programmed to simulate a single 64 channel data bus.

The field memories are divided into tables, each table set from 1 word to 32K words. A total of 100 tables may be defined. Once the tables and table lengths are defined, the field memories are loaded with appropriate test data (reference section 6.0, BE-64-VXI Command Description).

The maximum data rate of the field memories is 25 MHz

### 4.4.2. Timing Set Memories

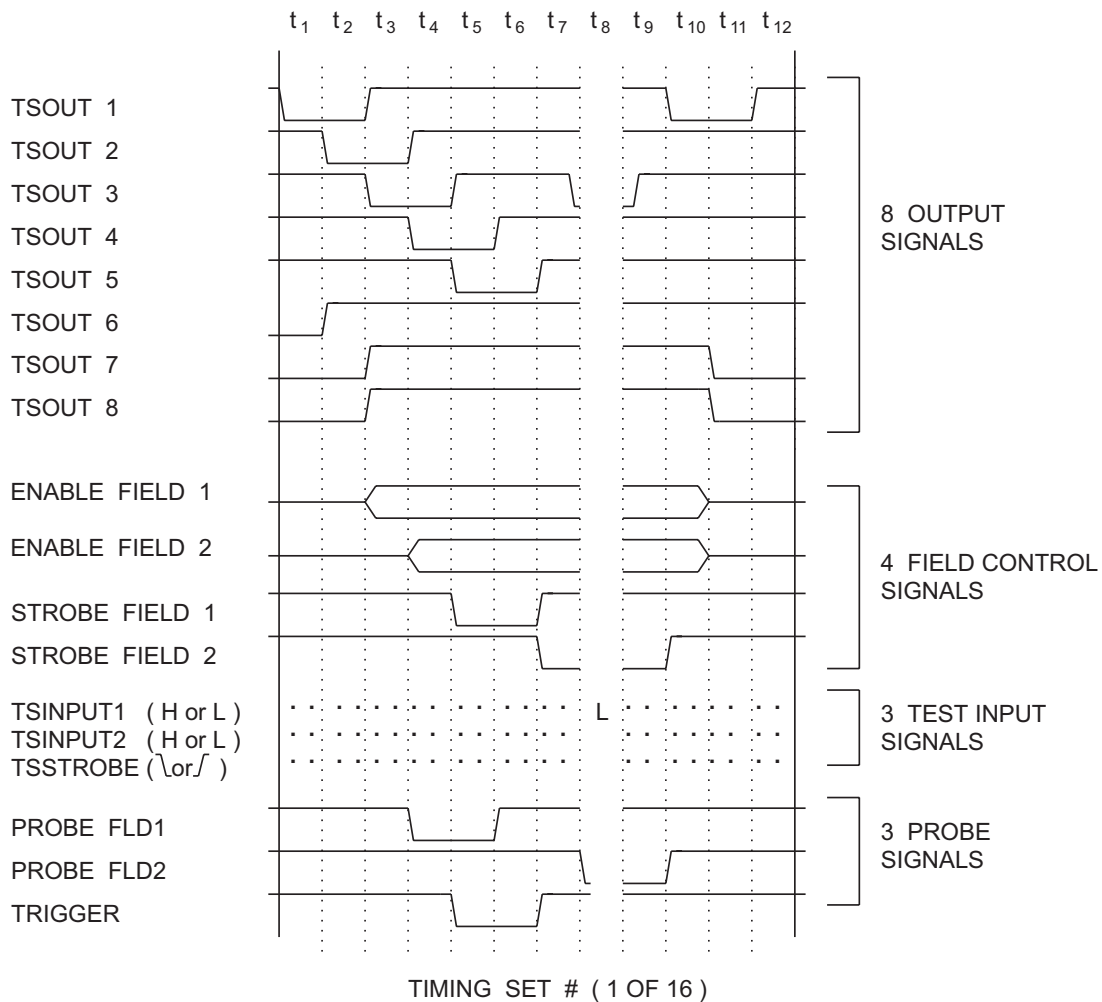
The BE-64 incorporates a total of 16 timing set memories, each timing set being 256 words by 32 bits wide.

Timing set #1 is dedicated to the idle timing set. On power-up, the idle timing set is programmed for two cells with all cells set to the high state. This state appears to be “no signal activity” for all outputs to the UUT. If the user desires an “active” idle timing set, the idle timing set can be programmed to any state desired. For example, if the BE-64 was used to simulate a 68020 microprocessor, it may be desirable to simulate a “READ FROM ROM” cycle during the idle time.

A minimum of one timing set and a maximum of 15 timing sets (excluding the idle timing set) must be programmed prior to executing a useful bus emulator command. The format for the timing set data can be found in section 6.0, BE-64 VXI Command Description.

### 4.4.3. Timing Sets

Fig. 24 depicts an example for signals programmed for one of the BE-64 sixteen timing sets.



**Figure 24**

The timing set signals are defined as follows.

- 1) TSOUT1 thru TSOUT8: Eight user defined timing signals
- 2) ENABLE FIELD 1, ENABLE FIELD 2: Enable signals for FIELD 1 and FIELD 2 data buses
- 3) STROBE FIELD 1, STROBE FIELD 2: Strobe signals for FIELD 1 and FIELD 2 data buses
- 4) TSINPUT1, TSINPUT2: Input signals to the timing set from the UUT. These signals can be tested for either a logic high or logic low condition. Multiple tests can occur within a timing set.
- 5) TSSTROBE: Input signal to the timing set from the UUT. This signal can be tested for a high to low transition or a low to high transition. Multiple test can occur within a timing set.

PROBE FLD1, PROBE FLD2: These two signals can be gated to the VXI TTLTRG signals and are used in conjunction with Talon's VXI signature/logic analyzer module.

TRIGGER: The trigger signal is gated with a TABLE, WORD and LOOP SYNC signal. This composite signal is gated to the VXI TTLTRG signals and is used in conjunction with Talon's VXI signature/logic analyzer module. This signal is also available on the front panel BNC.

Each timing set is clocked by a 50 MHz clock (20 nsec period), 20 MHz clock (50 nsec period), 10 MHz clock (100 nsec period) or an external clock ( 50 MHz). Each timing set has a minimum of 2 cells and a maximum of 256 cells.

During a "test cell" (TSINPUT1, TSINPUT2, or TSSTROBE) a timeout value may be defined. The time-out is programmable from 40 nsec to 640 usec. When enabled, the time-out logic will force the tested condition true, inform the VXI controller a time-out occurred and light the time-out LED on the front panel.

In addition to the programmed time-out function, any cell can be programmed with an inserted delay from 40 nsec to 640 us.

#### 4.4.4. Sequence Logic

Once the field memories and the timing set memories are loaded, the user can define a sequence of operations to be executed. A total of 16 sequences, plus the idle sequence, can be defined.

Each sequence, including the idle sequence, includes the following parameters.

1. defines a particular timing set.
2. defines a field table # (the table # includes the table length).
3. defines a loop count for the defined table (loop count = 1 through 64K or continuous) (the idle sequence is automatically set to an infinite loop).

Typically, the BE-64 would be continuously running with the idle sequence executing the idle timing set. Upon VXI command, the BE-64 is commanded to execute from 1 to 16 sequences, each sequence defining a timing set, table # and loop count. The first sequence does not start until the completion of the current idle sequence.

Each sequence, defining a timing set and table #, can be programmed to run for one loop or up to 64K loops. When looping, there is zero delay time between the last word of the table and the first word of the table. When all tables are complete, the next sequence is executed and again there is zero delay time between the last word of sequence n and the first word to sequence n+1. Likewise, when returning to the idle cycle, there is zero delay between sequences.

Any of the 16 sequences can be programmed to run continuously. Once a sequence is running continuously, it will remain running until commanded to complete via a VXI command. When commanded to complete, the sequence will complete all words in the given table before continuing to the next sequence or to the idle sequence.

Additionally, the list of sequences can be commanded to run continuously. In this mode, the last defined sequence will be followed by the first defined sequence without returning to the idle sequence. The sequence will continue in this mode until commanded to stop by one of two VXI commands. One VXI stop command will allow all sequences to continue being executed until the last loop of the last word of the last sequence is detected. At this time, the BE-64 returns to the idle sequence. This is referred to as a synchronous stop.

The other VXI stop command immediately stops the sequence and causes an immediate return to the idle sequence.

## 5. I/O SIGNAL DESCRIPTION

## 5.1. Program I/O

### 5.1.1. PI/O

PIO1 (0-7) (8 lines) [J1-(1,3,5,7,9,11,13,15)B]: The PIO1 lines are set to be either input or output in an eight bit group. Each line can be either set or reset by the VXI controller when set to output mode, or may be tested for a high or low condition when in input mode. On power up or system reset, the PIO1 lines are set to the input mode.

PIO2 (0-7) (8 lines) [J1-(17,19,21,23)B, J3-(25,27,29,31)B]: Same function as the PIO1 lines.

PIO CONTROL LINES (2 lines):

PIOEN- [J1-25B]: The PIOEN- input line enables the PIO1 and PIO2 lines when they are set to the output mode (PIOEN- = Low = Enable, PIOEN- = High = Tristate).

PIOSTB- [J1-27B]: The PIOSTB- input line strobes the PIO1 and/or PIO2 input register when they are set to the input mode (strobe occurs on positive to negative edge).

### 5.1.2. Counter Output

OUT (0-7) (8 lines) [J4-(9,11,13,15,17,19,21,23)B]: The OUT 0-7 lines can be set to be either an output register (identical to the PIO lines when in output mode) or they can be set up to be an eight bit counter. When in the counter mode, the control lines are compatible with the field memory control lines (see Proprietary Control Signals, section 5.2.8). With proper connection the OUT 0-7 lines can be used to simulate the MSB's of an address bus. This allows memory testing of cards with 16 megabyte of RAM, with zero delay between continuous 16 MEG address boundaries.

OUT CONTROL LINES (6 lines):

OUTEN- [J4-25B]: The OUTEN- input line enables the OUT 0 thru 7 lines (OUTEN- = Low = Enable, OUTEN- = High = Tristate).

CNTCK- [J3-1A]: The CNTCK- input signal clocks the output counter when in counter mode (clock occurs on positive to negative edge).

CNTEN- [J3-3A]: The CNTEN- input signal enables the output counter to advance the count at the next clock (counter advances on CNTEN- = Low).

CNTLD- [J3-5A]: THE CNTLD- input signal enables the counter to load with the initial value at the next CNTEN- signal and CNTCK-clock signal. (counter loads when CNTLD- = Low).

UP/DN- [J3-7A]: The UP/DN- input signal defines the counter to be either an UP or DOWN counter (UP/DN- = Low = Down Count).

OUTCAR- [J3-11A]: The OUTCAR- output signal indicates the count value of hex FF (UP/DN- = 1) or hex 00 (UP/DN- = 0)

## 5.2. Timing Set Out Signals

### 5.2.1. Timing Set Output Signals

TSOUT (1-8) (8 lines) [J1-(1,3,5,7,9,11)A, J3-(19,21)A]: The eight TSOUT output signals are general purpose programmable signals available for the UUT or test fixture interface. They are programmed to a high or low level with 20 nsec resolution.

### 5.2.2. Timing Set Test Signals

TSINPUT1,2 [J1-(13,15)A]: The two TSINPUT input signals can be sampled by the timing set. They can be tested for either a logic "0" or a logic "1" state.

If the tested condition is true, the timing set advances to the next state. If the tested condition is false, the timing set enters a "WAIT" state. It remains in the "WAIT" state until either the tested condition becomes true or until the programmable time-out function is detected.

The TSINPUT signals allow the timing set to "handshake" with the UUT.

TSSTROBE [J1-17A]: The TSSTROBE input signal is similar in function to the TSINPUT signals with the exception that the timing set tests for the occurrence of either a positive or negative edge on the TSSTROBE input signal.

The edge detection logic is reset for the following conditions.

- 1) during an IDLE cycle.
- 2) immediately after a tested true condition is detected.
- 3) at the last cell position.

Therefore, an edge can be detected after the start of the timing set and multiple edges can be detected.

The detection of a positive edge does not affect the negative edge logic, and vice versa.

TSSTROBE can also be jumpered (E4-E5) so that an internal signal, identical to TTLTRGA, will be the source.

### 5.2.3. Timing Set Field Control Signals

ENABLE FIELD 1: The ENABLE FIELD 1 signal programmed in the timing set is not routed to the front panel I/O lines.

When selected, and when in output mode, the ENABLE FIELD 1 signal forces field 1 (UUT ADDRESS bus) from tri-state to an active state.

STROBE FIELD 1: The STROBE FIELD 1 signal, programmed in the timing set, is not routed to the front panel I/O lines.

When selected by the output register of FIELD 1 (UUT ADDRESS bus), the STROBE FIELD 1 signal strobes the data from the 32K x 32 bit memory into the output register. The data transfer occurs on the positive to negative transition of the STROBE FIELD 1 signal.

When selected by the input register of FIELD 1 (UUT ADDRESS bus), the STROBE FIELD 1 signal strobes the data on the FIELD 1 bus into the input register. The data transfer occurs on the positive to negative transition of the STROBE FIELD 1 signal.

ENABLE FIELD 2: The ENABLE FIELD 2 signal programmed in the timing set is not routed to the front panel I/O lines.

When selected, and when in output mode, the ENABLE FIELD 2 signal forces field 2 (UUT DATA bus) from tri-state to an active state.

STROBE FIELD 2: The STROBE FIELD 2 signal, programmed in the timing set, is not routed to the front panel I/O lines.

When selected by the output register of FIELD 2 (UUT DATA bus), the STROBE FIELD 2 signal strobes the data from the 32K x 32 bit memory into the output register. The data transfer occurs on the positive to negative transition of the STROBE FIELD 2 signal.

When selected by the input register of FIELD 2 (UUT DATA bus), the STROBE FIELD 2 signal strobes the data on the FIELD 2 bus into the input register. The data transfer occurs on the positive to negative transition of the STROBE FIELD 2 signal.

#### 5.2.4. Timing Set Probe Signals

PROBE FLD1: The PROBE FLD1 signal generates a pulse compatible with Talon's VXI signature/logic analyzer probe. The user should program this signal within the enable time of the ENAB FLD1 signal. The PROBE FLD1 signal can be routed to the TTLTRG signals on the VXI bus.

PROBE FLD2: The PROBE FLD2 signal generates a pulse compatible with Talon's VXI signature/logic analyzer probe. The user should program this signal within the enable time of the ENAB FLD2 signal. The PROBE FLD2 signal can be routed to the TTLTRG signals on the VXI bus.

TRIGGER: The TRIGGER signal is gated with the memory table sync signal. This combinatorial signal, compatible with Talon's VXI signature/logic analyzer probe, generates the trigger signal used by the logic analyzer function. The trigger function occurs at the detection of a logic "0" on the TRIGGER signal. The TRIGGER signal is also available on the front panel BNC. The TRIGGER signal can be routed to the TTLTRG signals on the VXI bus.

#### 5.2.5. Timing Set Misc. Control Signals

CYCLE- (1 line) [J1-33B]: The CYCLE- output signal, when low, indicates a non-idle cycle is being executed.

CYCL 0,1,2,3 (4 lines) [J3-(17,19,21,23)B]: The CYCL 0,1,2,3 output signals are a binary value defining the present timing set. Hex zero indicates the idle timing set.

DATR/W- (1 line) [J1-27A]: A low on the DATR/W- output signal indicates an active timing set #2 (WRITE MEMORY) or timing set #3 (WRITE I/O). This signal may be used to generate the R/W- control line of a UUT interface.

MI/O- (1 line) [J1-29A]: A low on the MI/O- output signal indicates an active timing set #3 (WRITE I/O) or timing set #5 (READ I/O). This signal may be used to generate the memory/I/O control signal for Intel microprocessors.

INTCYC- (1 line) [J1-33A]: A low on the INTCYC- output signal indicates an active timing set #6 (INTERRUPT CYCLE). This signal indicates an active interrupt acknowledge cycle is being executed.

BUSTST- (1 line) [J1-31A]: A low on the BUSTST- output signal indicates an active timing set #7 (BUS TEST). This signal may be used to indicate to the UUT that a bus test cycle is being executed.

TSCLK-A (1 line) [J1-35B]: The TSCLK-A output signal is the present clock driving the timing set. Timing set signals are activated at the high to low transition of this signal.

### 5.2.6. Bus Arbitration Signals

BUSREQ- (1 line) [J1-29B]: the BUSREQ-input signal requests the bus emulator to enter a tri-state condition with an active Low state. The bus emulator will enter the tri-state condition when BUSREQ- is active (and enabled by a VXI command) and immediately after the last bit of the present timing set cycle.

BUSACK- (1 line) [J1-31B]: The BUSACK- output signal goes active Low indicating the bus emulator has acknowledged the present bus request (BUSREQ-). The bus emulator enters a hold state and appropriate output signals are tri-stated. BUSACK- goes not true (high) immediately after the BUSREQ- goes not true (high) and after syncing up to the timing set clock.

UUTCLP- (1 line) [J1-39A]: A low on the UUTCLP- input signal indicates a test connector has been clipped over the UUT microprocessor.

### 5.2.7. Timing Set External Clock

EXCLK- (1 line) [J1-25]: The EXCLOCK-input signal is the user defined external clock which may be selected to drive the timing sets. The maximum frequency is 50 MHz. The timing set signals are activated at the high to low transition of the EXCLK- clock.

### 5.2.8. Proprietary Control Signals

The BE-64 board has been designed to simulate any digital interface and in particular bus structured interfaces. To effectively simulate the latest Intel and Motorola microprocessors at clock speeds of 50 MHz, several signals are required which Talon considers proprietary.

The BE-64 can drive a parallel to serial converter card which achieves data rates to 100 MHz. All the necessary control signals for the conversion card reside in these proprietary control signals.

In addition, several control lines from the field memory address logic are output which are compatible with the OUT 0-7 counter function.

### 5.2.9. External Sequence Stop Control

STOPSEQ- (1 line) [J3-9A]: An active low pulse, greater than 50 nsec, on input signal STOPSEQ- will cause a sequence to stop. The VXI controller can verify the sequence properly stopped. Use with caution if the user is uncertain where in the sequence STOPSEQ- is activated.

### 5.2.10. Sequence State Output Signals

LSTBIT- (1 line) [J3-13A]: The LSTBIT- output signal is active low during the last cell of the current timing set. Note: Not active during the idle timing set.

LSTWRD- (1 line) [J3-15A]: The LSTWRD- output signal is active low during the last word of the current table. LSTWRD- stays low for as long as one execution of the timing set. Note: Not active during the idle timing set.

LSTXFB- (1 line) [J3-17A]: The LSTXFB- output signal is active low during the last word of the last loop of a table. LSTXFB- stays low during the entire timing set. Note: Not active during the idle timing set.

## 5.3. Field Control Signals

### 5.3.1. Field Signals

FLD1 (0-31)(FIELD1, (uut ADDRESS BUS)) (32 lines) [j2(1,3,.....,39)A, J2 (1,3.5.7)B, J4(1,3...,15)A ALL ODD]: The FLD1-0 thru FLD1-31 signals are bi-directional signals with 32K bits behind each channel. The maximum data rate for this field is 25 MHz. This field may be used to simulate an address bus of the UUT. However, it is general purpose and may be used for any UUT function.

F1DIROUT- (1 line) [J4-31B]: The F1DIROUT- input signal defines the direction of FIELD 1 when FIELD 1 is set in external mode. FIELD 1 is set to the OUTPUT direction when F1DIROUT- = Low.

F1ENAB- (1 line) [J4-33B]: The F1ENAB- input signal enables FIELD 1 data when FIELD 1 is set in the external mode. FIELD 1 data is enabled when F1ENAB- = Low. FIELD 1 data is enabled only if the direction is set to be output.

STBFLD1- (1 line) [J1-35A]: When selected for the input register, the STBFLD1- input signal strobes FIELD 1 data into FIELD 1 input register. When selected for the output register, the STBFLD1- signal strobes FIELD 1 output data into the output register. The data is strobed on the high to low transition of the STBFLD1- signal.

F1ENABED- (1 line) [J3-33B]: The F1ENABED- output signal is active low whenever FIELD 1 (UUT ADDRESS BUS) is in the output mode and the enable signal is true.

FLD2 (0-31) (FIELD 2, (UUT DATA BUS)) (32 lines) [J2(9,11,....,39)B, J4(17,19,...39)A, J4(1,3,5,7)B ALL ODD]: The FLD2-0 thru FLD2-31 signals are bi-directional signals with 32K bits behind each channel. The maximum data rate for this field is 25 MHz. This field may be used to simulate a data bus of the UUT. However, it is general purpose and may be used for any UUT function.

F2DIROUT- (1 line) [J4-35B]: The F2DIROUT- input signal defines the direction of FIELD 2 when FIELD 2 is set in external mode. FIELD 2 is set to the OUTPUT direction when F2DIROUT- = Low.

F2ENAB- (1 line) [J4-37B]: The F2ENAB- input signal enables FIELD 2 data when FIELD 2 is set in the external mode. FIELD 2 data is enabled when F2ENAB- = Low. FIELD 2 data is only enabled if the direction is set to be output.

STBFLD2- (1 line) [J1-37A]: When selected for the input register, the STBFLD2- input signal strobes FIELD 2 data into FIELD 2 input register. When selected for the output register, the STBFLD2- signal strobes FIELD 2 output data into the output register. The data is strobed on the high to low transition of the STBFLD2- signal.

F2ENABED- (1 line) [J3-35B]: The F2ENABED- output signal is active low whenever FIELD 2 (UUT DATA BUS) is in the output mode and the enable signal is true.

### 5.3.2. Byte Enable Signals

BE0-,1-,2-,3- (4 lines) [J1-(19,21)A, J4-(27,29)B]: Most bus and microprocessor structured interfaces have separate control lines to indicate the present size of the data bus (byte, word, or longword). Moreover, byte and word transfers may be defined to be in the LSB or MSB positions. The byte enable output signals are defined by respective VXI compatible commands. The active condition of the BE0- thru BE3- is defined by the present transfer type (byte, word, or longword), as well as Bit 0 and Bit 1 of Field 1 (which represents A0 and A1 of the address bus). These signals are further qualified by timing set signal #8 (TSOUT8).

### 5.3.3. Bus Emulator Output Clock

CLOCK-B (1 line) [J3-29A]: The CLOCK-B output signal is the currently selected clock rate for the bus emulator.

## 5.4. VXI TTL Trigger Signals

### 5.4.1. TTL Trigger Source Selection

TTLTRGA (1 line) [J3-33A]: The TTLTRGA output signal is user defined to select any one of the TTLTRG (0-7) lines as the source. TTLTRGA can also be defined to be in a tri-state condition.

TTLTRGB (1 line) [J3-35A]: The TTLTRGB output signal is similar in function to the TTLTRGA signal. TTLTRGB can also be jumpered to TSTEST2 (E2-E3). This jumper is not normally installed.

### 5.4.2. TTL Trigger Output Selection

PRBDAT- (1 line) [J1-23A]: The PRBDAT- input signal is a user defined probe signal. PRBDAT- can be routed to the VXI trigger lines TTLTRG (4-7).

## 5.5. Self Test Fixture Signals

### 5.5.1. Self Test Input Signal

SELFT- (1 line) [J3-27A]: The SELFT- input signal is used by the self test fixture. Do not use.

### 5.5.2. Self Test Output Signals

STSTB- (1 line) [J3-25A]: The STSTB- output signal is used to clock the self test fixture. Not to be used by the user.

STSTB-1 (1 line) [J3-31A]: Same function as STSTB-.

## 5.6. Miscellaneous Signals

### 5.6.1. Reset Signal

UUTRST- is low for a minimum of 50 milliseconds and is asynchronous.

### 5.6.2. UUT Power On Signal

UUT5V+ (1 line) [J1-39B]: A TTL logic "0" on input line UUT5V+ indicates there is no power on the UUT. A TTL logic "1" on UUT5V+ indicates there is power on the UUT. UUT5V+ is pulled low through a 10K resistor.

### 5.6.3. Additional Power Lines From VXI Backplane

SELV+ (1 line) [J3- 98]: The SELV + output line is user defined to connect to either the +12V (E65-E66) or +24V (E67-E66) from the VXI backplane (unfused). Use with caution.

SELV- (1 line) [J3-11B]: The SELV- output line is user defined to connect to either the -12V (E68-E69) or -24V (E70-E69) from the VXI backplane (unfused). Use with caution.

## 6. BE-64 VXI COMMAND DESCRIPTION

Available Upon Request